Amendments to the Abstract:

Please replace the Abstract at page 19 with the following amended abstract:

--ABSTRACT OF THE DISCLOSURE

An integrated semiconductor memory ~~having~~ with selection transistors ~~can be~~ is formed at a ridge ~~web. The web ridge can be~~ arranged on an insulation layer. The first source/drain region ~~can be~~ is arranged on the insulation layer at one lateral end of the [[web]] ridge and the second source/drain region ~~can be~~ is arranged on the insulation layer at another lateral end of the [[web]] ridge. The longitudinal sides of the [[web]] ridge and a top side of the [[web]] ridge ~~can be~~ is covered with a layer sequence including a gate dielectric and a gate electrode. ~~High write-read currents can be achieved in the on-state of the selection transistors and leakage currents occurring in the off state can be reduced.~~